AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A method for forming an electronic device in a multilayer structure comprising the steps of:

~~defining a topographic profile in a laterally extending first layer~~ depositing a first layer in such a way as to define one or more electrodes of the device and a topographic profile;

depositing at least one non-planarizing layer on top of the first layer such that the topographic profile of the surface of the at least one ~~or each~~ non-planarizing layer conforms to that of the laterally extending first layer; and

depositing a pattern of at least one additional layer onto the top-most non-planarizing layer to define one or more elements of the device, such that the lateral location of the additional layer is defined by the shape of the topographic profile of the non-planarizing layer, and whereby the additional layer is laterally aligned with the topographic profile in the first layer.

2. (original): A method as claimed in claim 1, wherein the additional layer is deposited from solution.

3. (previously presented): A method as claimed in claim 1, wherein prior to the step of depositing the additional layer, the method further comprises the step of performing a surface modification process that has a different effect on relatively raised regions of the non-planarizing layer in comparison to relatively depressed regions of the non-planarizing layer, so as to generate a surface energy contrast between the relatively raised and relatively depressed regions of the non-planarizing layer.

4. (original): A method as claimed in claim 3, wherein the surface modification process comprises selectively depositing a surface modification material which modifies the surface energy of the substrate.

5. (previously presented): A method as claimed in claim 1, wherein the substrate comprises a flexible plastic substrate such as poly(ethleneterephtalate) (PET), polyethersulphone (PES) or polyethernaphtalene (PEN).

6. (previously presented): A method as claimed in claim 3, wherein the step of performing a surface modification process comprises laminating the surface of the substrate by bringing the surface into contact with a flat stamp bearing a surface modification material.

7. (original): A method as claimed in claim 6, wherein the surface modification material is a self assembled monolayer (SAM).

8. (previously presented): A method as claimed in claim 6, wherein the SAM is able to bond to a functional group on the surface, and has a tail containing a polar group.

9. (previously presented): A method as claimed in claim 1, wherein the non-planarizing layers are deposited by vacuum deposition techniques.

10. (previously presented): A method as claimed in claim 1, wherein the non-planarizing layers are deposited from solution.

11. (original): A method as claimed in claim 6, further comprising the step of applying a mechanical support layer to the surface of the non-planarizing layer in order to maintain separation of the flat stamp and relatively depressed regions of the non-planarizing layer during the step of performing a surface modification process.

12. - 18. (canceled).

19. (previously amended): A method as claimed in claim 1, wherein prior to the step of depositing at least one additional layer, the method further comprises the step of applying a surface modification layer on one of the relatively raised or relatively lowered regions of the top-most non-planarizing layer such that the additional layer is confined to the other of the relatively raised or relatively lowered regions of the top-most non-planarizing layer.

20. (original): A method as claimed in claim 19, wherein prior to the step of applying a surface modification layer, a surface treatment step is applied selectively to one of the relatively raised or relatively lowered regions of the non-planarizing layer.

21. (previously presented): A method as claimed in claim 19, wherein the surface treatment step comprises a step in which the additional non-planarizing layer is made wetting for the deposition of the additional layer.

22. (previously presented): A method as claimed in claim 19, wherein the surface modification layer is a low surface energy polymer.

23. (previously presented): A method as claimed in claim 3, wherein the step of performing a surface modification process comprises depositing a surface modification material onto the substrate at an oblique angle such that the surface modifying material is deposited onto the raised portions of the substrate, and the depressed portions are shadowed by the raised portions during the deposition of the surface modification material.

24. (original): A method as claimed in claim 23, wherein the low surface energy polymer is a fluoropolymer.

25. (previously presented): A method as claimed in claim 1, wherein the additional layer forms an electrically functional element of the electronic device.

26. (previously presented): A method as claimed in claim 19, wherein the surface energy of surface modification layer is modified according to a topographic profile of the surface modification layer.

27. - 32. (canceled).

33. (currently amended): A method as claimed in claim ~~32~~ 1, wherein the first layer defines ~~functional element is~~ a gate electrode of the electronic device.

34. (currently amended): A method as claimed in claim 1, wherein the pattern of the at least one additional layer deposited onto the non-planarizing layer comprises source and drain electrodes ~~at least one functional element~~ of the electronic device.

35. (canceled).

36. (currently amended): A method as claimed in claim ~~32~~ 1, wherein the first layer defines ~~at least one functional element comprises~~ a source and a drain electrode of the electronic device.

37. (currently amended): A method as claimed in claim 1, wherein the pattern of the at least one additional layer deposited onto the non-planarizing layer comprises a gate electrode ~~functional element~~ of the electronic device.

38. (canceled).

39. (previously presented): A method as claimed in claim 1, wherein the electronic device is a transistor.

40. (previously presented): A method as claimed in claim 1, wherein the step of depositing at least one non-planarizing layer comprises depositing a first non-planarizing layer and a second non-planarizing layer.

41. (original): A method as claimed in claim 40, wherein the first non-planarizing layer is a semiconductor layer.

42. (previously presented): A method as claimed in claim 41, wherein the second non-planarizing layer is a dielectric layer.

43. (original): A method as claimed in claim 42, wherein the dielectric layer is a gate dielectric layer.

44. (previously presented): A method as claimed in claim 1, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 10 μm.

45. (previously presented): A method as claimed in claim 1, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 5 μm.

46. (previously presented): A method as claimed in claim 1, wherein the additional layer is laterally aligned with the topographic profile in the first layer such that a lateral overlap between edges of the additional layer and boundaries of the topographic profile in the first layer to which the additional layer is confined is less than 1 μm.

47. (previously presented): A method as claimed in claim 3, wherein the step of performing a surface modification process on a surface having a topographic profile comprising at least one relatively raised region and at least one relatively depressed region, comprises:

depositing a planarizing sacrificial layer over the topographic profile;

etching the surface of the sacrificial layer to reveal the relatively raised regions of the surface, but leaving the relatively depressed regions covered by the sacrificial layer, so as to define a layer having a substantially planar upper surface;

performing a surface energy modification process on the surface layer; and

removing the remaining areas of the sacrificial layer to reveal the depressed regions.

48. (original): A method as claimed in claim 47, wherein the planarizing sacrificial layer is deposited by spin coating.

49. (previously presented): A method as claimed in claim 47, wherein the planarizing sacrificial layer is deposited by a polymer solution.

50. (original): A method as claimed in claim 49, wherein the polymer solution is an organic based polymer solution containing siloxane.

51. (previously presented): A method as claimed in claim 47, wherein the etching step comprises an oxygen plasma etching step.

52. (previously presented): A method as claimed in claim 47, wherein the step of performing a surface energy modification process on the surface layer, comprises exposing the surface layer to a vapor of a self-assembling molecule.

53. (previously presented): A method as claimed in claim 47, wherein the step of removing the remaining areas of the sacrificial layer comprises washing the substrate in a solvent in which the sacrificial layer is soluble, but in which the surface layer is insoluble.